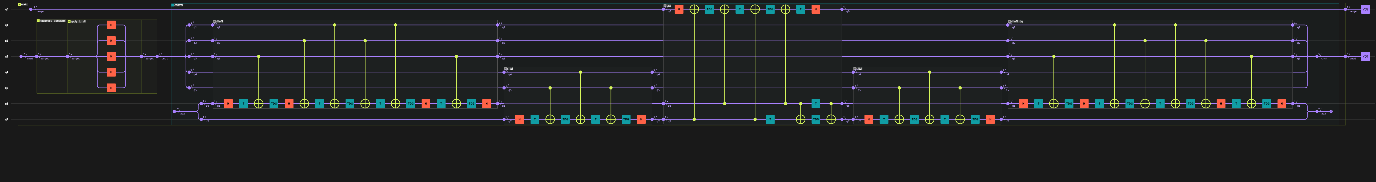
**Overview**

This document presents three different implementations of a Multiple-Control X (MCX) gate with 5 control qubits and 1 target qubit. Each implementation optimizes for different metrics: circuit depth, quantum register width, or a balanced approach between the two.

**Minimized Depth:**

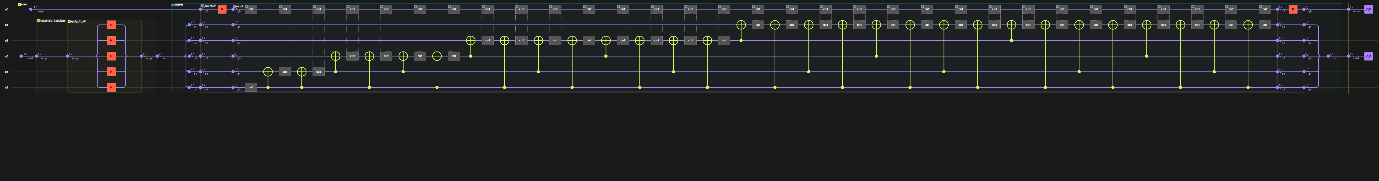


Depth: 34

Implementation details:

* Uses parallel decomposition of the multi-control operation
* Employs additional qubits to reduce sequential operations
* Achieves minimal circuit depth through parallel execution paths
* Trade-off: Requires more physical qubits to achieve the depth optimization

**Minimized Width:**



Width: 6

Implementation details:

* Uses basic decomposition into sequential Toffoli gates
* Requires no additional qubits
* Operates strictly on the input qubits (5 controls + 1 target)
* Trade-off: Increased circuit depth due to sequential operations

**Somewhere in between:**

A screenshot of a video game

Description automatically generated

Depth: 34 , Width: 8

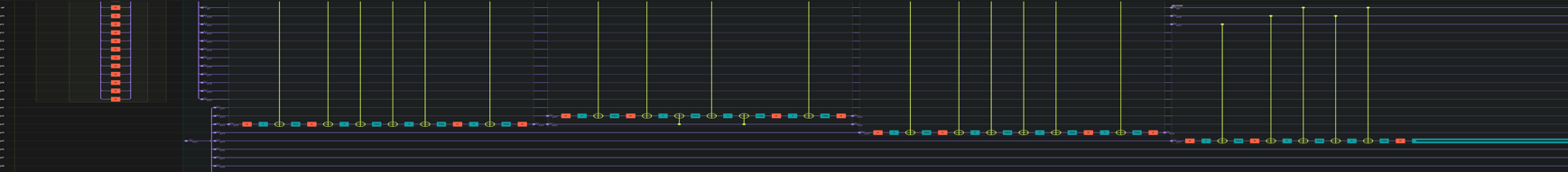
Implementation details:

* Uses limited qubits for partial parallelization
* Achieves the same depth as the fully optimized version
* Reduces qubit requirements compared to depth-optimized version
* Trade-off: Good balance between resource requirements

**Resource Trade-offs**

1. Depth vs. Width:
   * Lower depth generally requires more qubits
   * Fewer qubits leads to increased circuit depth
   * The balanced implementation shows that optimal depth can be achieved with fewer resources than the maximum
2. Implementation Complexity:
   * Width-optimized version is simpler but slower
   * Depth-optimized version requires more complex control logic
   * Balanced version maintains complexity similar to depth-optimized but with fewer resources

Mcx with 20 cntrl qbits and 1 target:

Optimize depth:  


Depth:66 width 30

Optimize width:

Depth:1894 width 22

A Multiple-Control X (MCX) gate with 20 control qubits and 1 target qubit for 22 to 30 qbits.

width: 22 depth: 1894

width: 23 depth: 1427

width: 24 depth: 1079

width: 25 depth: 893

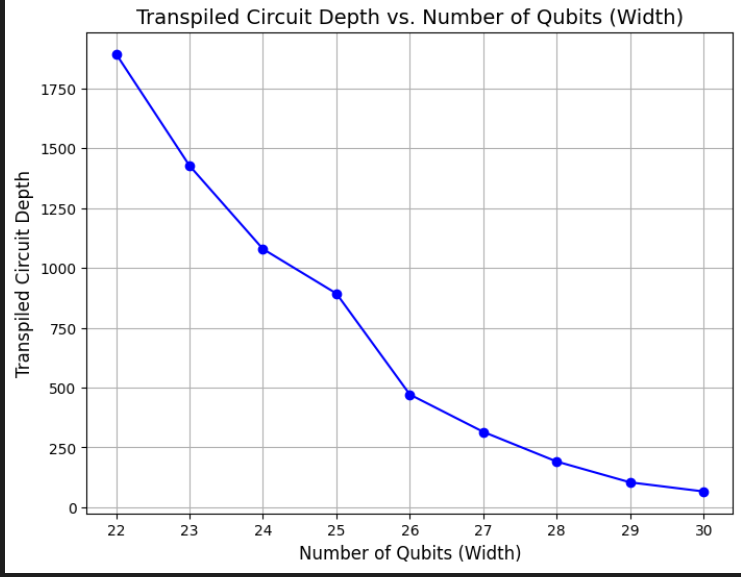
width: 26 depth: 471

width: 27 depth: 315

width: 28 depth: 191

width: 29 depth: 104

width: 30 depth: 66



As we can see in the graph as we increase the number of qubits (width) from 22 to 30, we see a clear inverse relationship with circuit depth. The 22 qubits implementation is best for systems with very limited qubit availability but can handle deeper circuits, though the depth will be significantly higher at 1894. At the other end, using 30 qubits achieves a very low depth of 66 but requires substantially more spatial resources.

The most balanced approach is to choose a width of 25-26 qubits, which results in a depth of around 471-893. This configuration is ideal when working with mid-range quantum hardware, as it provides reasonable performance without requiring maximal resources. This middle-ground approach offers a practical trade-off between resource usage and circuit complexity, making it suitable for many real-world implementations where both qubit count and circuit depth need to be optimized.

The data clearly shows that increasing the circuit width leads to exponential reductions in circuit depth. However, this comes at the cost of requiring more qubits, which may not always be available or practical. The balanced implementation with 25-26 qubits represents a sweet spot that balances these competing demands, offering a practical solution for most quantum computing applications where both resource efficiency and performance are important considerations.